Amendments to the Claims:

Please amend claims 1-3 as follows. Please add new claims 9-21 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A method of fabricating a local interconnection comprising:

forming a selective epitaxial growth seed layer pattern on a region of a semiconductor substrate where a local interconnection is to be formed, the region including an active region on which a gate is formed;

forming a selective epitaxial layer on the selective epitaxial growth seed layer pattern, on a top surface of the gate, and on an exposed surface of the semiconductor substrate by performing epitaxial growth on the resultant structure; and

reducing a resistance of the selective epitaxial layer to complete the local interconnection.

2. (currently amended) The method of claim 1, further comprising, prior to forming the selective epitaxial growth seed layer pattern:

forming a shallow trench isolation structure on the semiconductor substrate to define [[an]]the active region;

forming [[a]]the gate on the active region; and

forming a spacer on a sidewall of the gate, and

wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed layer pattern on the shallow trench isolation structure, and forming the selective epitaxial layer comprises forming the selective epitaxial layer on the active region, the selective epitaxial growth seed layer pattern, and the gate, and

wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a source/drain region of an adjacent transistor.

3. (currently amended) The method of claim 1, further comprising, prior to forming the selective epitaxial growth seed layer pattern:

forming a shallow trench isolation structure on the semiconductor substrate to define [[an]]the active region;

forming the gate to comprise first and second adjacent gates on the active region;

forming a spacer on sidewalls of the first and second gates; and

forming an insulating layer pattern for exposing an active region adjacent the first gate and exposing the second gate, and

wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed layer pattern on the insulating layer pattern, and forming the selective epitaxial layer comprises forming the selective epitaxial layer on the active region adjacent the first gate, the selective epitaxial growth seed layer pattern, and the second gate, and

wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a gate of an adjacent transistor.

4. (original) The method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by implanting ions into the selective epitaxial layer.

5. (original) The method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by siliciding the selective epitaxial layer.

6. (original) The method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises:

implanting ions into the selective epitaxial layer; and

siliciding the selective epitaxial layer.

7. (original) The method of claim 1, wherein the selective epitaxial growth seed layer pattern comprises an $Si_xO_yN_z$ layer pattern.

8. (original) The method of claim 7, wherein the selective epitaxial growth seed layer pattern comprises an $Si_xO_yN_z$ layer pattern, and wherein x is 55, y is 15, and z is 30.

9. (new) A method of fabricating a local interconnection comprising:

forming a selective epitaxial growth seed layer pattern on a region of a semiconductor substrate where a local interconnection is to be formed;

forming a selective epitaxial layer by performing epitaxial growth on the resultant structure; and

reducing a resistance of the selective epitaxial layer to complete the local interconnection, and further comprising, prior to forming the selective epitaxial growth seed layer pattern:

forming a shallow trench isolation structure on the semiconductor substrate to define an active region;

forming first and second adjacent gates on the active region;

forming a spacer on sidewalls of the first and second gates; and

forming an insulating layer pattern for exposing an active region adjacent the first gate and exposing the second gate, and

wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed layer pattern on the insulating layer pattern, and forming the selective epitaxial layer comprises forming the selective epitaxial layer on the active region adjacent the first gate, the selective epitaxial growth seed layer pattern, and the second gate, and

wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a gate of an adjacent transistor.

10. (new) The method of claim 9, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by implanting ions into the selective epitaxial layer.

11. (new) The method of claim 9, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by siliciding the selective epitaxial layer.

12. (new) The method of claim 9, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises:

implanting ions into the selective epitaxial layer; and

siliciding the selective epitaxial layer.

13. (new) The method of claim 9, wherein the selective epitaxial growth seed layer pattern comprises an $Si_xO_yN_z$ layer pattern.

14. (new) The method of claim 13, wherein the selective epitaxial growth seed layer pattern comprises an $Si_xO_yN_z$ layer pattern, and wherein x is 55, y is 15, and z is 30.

15. (new) A method of fabricating a local interconnection comprising:

forming a selective epitaxial growth seed layer pattern on a region of a semiconductor substrate where a local interconnection is to be formed, wherein the selective epitaxial growth seed layer pattern comprises an $Si_xO_yN_z$ layer pattern;

forming a selective epitaxial layer by performing epitaxial growth on the resultant structure; and

reducing a resistance of the selective epitaxial layer to complete the local interconnection.

16. (new) The method of claim 15, wherein the selective epitaxial growth seed layer pattern comprises an $Si_xO_yN_z$ layer pattern, and wherein x is 55, y is 15, and z is 30.

17. (new) The method of claim 15, further comprising, prior to forming the selective epitaxial growth seed layer pattern:

forming a shallow trench isolation structure on the semiconductor substrate to define an active region;

forming a gate on the active region; and

forming a spacer on a sidewall of the gate, and

wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed layer pattern on the shallow trench isolation structure, and forming the selective epitaxial layer comprises forming the selective epitaxial layer on the active region, the selective epitaxial growth seed layer pattern, and the gate, and

wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a source/drain region of an adjacent transistor.

18. (new) The method of claim 15, further comprising, prior to forming the selective epitaxial growth seed layer pattern:

forming a shallow trench isolation structure on the semiconductor substrate to define an active region;

forming first and second adjacent gates on the active region;

forming a spacer on sidewalls of the first and second gates; and

forming an insulating layer pattern for exposing an active region adjacent the first gate and exposing the second gate, and

wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed layer pattern on the insulating layer pattern, and forming the selective epitaxial layer comprises forming the selective epitaxial layer on the active region adjacent the first gate, the selective epitaxial growth seed layer pattern, and the second gate, and

wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a gate of an adjacent transistor.

19. (new) The method of claim 15, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by implanting ions into the selective epitaxial layer.

20. (new) The method of claim 15, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by siliciding the selective epitaxial layer.

21. (new) The method of claim 15, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises:

implanting ions into the selective epitaxial layer; and

siliciding the selective epitaxial layer.